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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,254	09/11/2003	Eric D. Groen	X-1359 US	5349

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EXAMINER	
FILE, ERIN M	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,254	GROEN ET AL.	
	Examiner	Art Unit	
	Erin M. File	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23* is/are allowed.

6)☒ Claim(s) *1 and 3-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Regarding the 102 Rejection of Claims 1, 4, and 6 over Ducaroir.

The applicant claims:

> Ducaroir, however, does not teach each and every element of Applicants' independent claim 1. Namely, Ducaroir does not teach or suggest "recovering a plurality of recovered clock signals from a plurality of serial data" as positively claimed by the Applicants (p. 8, Remarks, lines 10-12).
>
> Ducaroir also does not teach each and every element of Applicants' independent claim 6. Namely, Ducaroir does not teach or suggest "using said plurality of recovered clock signals concurrently to perform processing functions" as positively claimed by the Applicants (p. 8, Remarks, lines 21-24).

Claim 1 does not contain any limitation directed toward recovering a plurality of recovered clock signals from a plurality of serial data. Similarly Claim 6 does not contain any limitation directed toward using said plurality of recovered clock signals concurrently to perform processing functions. Therefore the applicant's arguments (p. 8, 9, Remarks) that Ducaroir does not teach each and every element of independent claims 1, 4, and 6 because Ducaroir fails to teach recovering a plurality of clock signals is spurious.

2. Regarding the 102 Rejection of Claims 8, 9, 22, and 23 over Ducaroir.

The applicant claims:

> Ziegler, however, does not teach each and every element of Applicants' independent claim 8. Namely, Ziegler does not teach or suggest "using a plurality of recovered clock signals from a plurality of serial data and a reference signal" as positively claimed by the Applicants.

Claim 8 does not contain the limitation "using a plurality of recovered clock signals". Claim 8 does contain limitations directed toward a recovering a plurality of clock signals from a plurality of serial data streams, which Ziegler meets. See particularly paragraph [0022], lines 39-44, which discloses a first and second clock recovered from a first and second data stream. In a similar manner Ziegler meets the limitations of Claim 22. Claim 23 as amended is allowable over the prior art of record.

3. Regarding the 103 Rejection of Claim 3 over Ducaroir in view of Ziegler.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

4. Regarding the 103 Rejection of Claims 5, 10, 11, and 14-16 over Ducaroir in view of Jordan.

A copy of provisional application of the Jordan reference is included with this office action. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does

not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

5. Regarding the 103 Rejection of Claims 12, 13, 17, and 18 over Ducaroir in view of Jordan and Ziegler.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

6. Regarding the 103 Rejection of Claims 19-21 over Ziegler in view of Akita.

Applicant's arguments, see Remarks, filed 12/29/2006, with respect to the rejection(s) of claim(s) 19-21 under 35 U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Ziegler and Knapp.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Ducaroir et al. (U.S. Pub. No. 2001/0043648).

Claim 6, Ducaroir discloses:

- first circuitry for receiving first serial data and recovering a first recovered clock based on the first serial data, wherein the first circuitry provides the first recovered clock to a first clock based functionality ([0020], lines 16-18, 21-23);
- second circuitry for generating and providing a reference clock to a second clock based functionality ([0020], lines 14-16);
- the first and second clock based functionalities concurrently perform processing functions using the first recovered clock and the reference clock, respectively ([0020]).

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 8, 9, 22, 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Ziegler et al. (U.S. Pub. No. 2003/0112798).

Claim 8, circuitry for receiving a plurality of input serial data streams (Ziegler discloses receiving a first serial bit stream ([0021], lines 1-2 and receiving a second serial bit stream [0021], lines 4-5); clock data recovery circuitry for recovering a corresponding plurality of recovered clocks based on the plurality of input serial data streams; circuitry for providing a reference clock ([0029], lines 1-3); and logic for selecting from the plurality of input serial data streams and for providing at least one outgoing serial data stream to an outgoing transmit block (Ziegler discloses recovering a first recovered clock from the first serial bit stream [0023], lines 39-41 and recovering a second recovered clock from the second serial bit stream [0023], lines 42-44); wherein the logic provides each received input serial data stream of the plurality of input serial data streams to the outgoing transmit block based upon each corresponding recovered clock of the plurality of corresponding recovered clocks ([0021], lines 6-12).

Claim 9, Ziegler further discloses the outgoing transmit block is a transmitter port ([0021], lines 6-12).

Claim 22, Ziegler discloses receiving a first serial bit stream ([0021], lines 1-2) and recovering a first recovered clock from the first serial bit stream ([0023], lines 39-41); providing the first clock to a first circuit portion ([0029], line 5-7, A-FIFO-1314 is controlled by first extracted clock); receiving a second serial bit stream ([0021], lines 4-5) and recovering a second recovered clock from the second serial bit stream ([0023],

lines 42-44); providing the second clock to a second circuit portion ([0029], line 5-7, B-FIFO-1334 is controlled by second extracted clock); providing a reference clock to a third circuit portion ([0029], lines 1-3, A-FIFO-2318 and B-FIFO-2338 are controlled both by the same reference clock 322); and concurrently performing processing functions in the processing block using the first and second clocks and the reference clock ([0029], the read and write operations of both A and B FIFOs occur simultaneously).

Claim 23, Ziegler discloses receiving a plurality of input data streams (Ziegler discloses receiving a first serial bit stream ([0021], lines 1-2 and receiving a second serial bit stream [0021], lines 4-5); recovering a corresponding plurality of clocks based on the plurality of input data streams (Ziegler discloses recovering a first recovered clock from the first serial bit stream [0023], lines 39-41 and recovering a second recovered clock from the second serial bit stream ([0023], lines 42-44); determining at least one output port for providing outgoing data streams ([002], lines 6-12); and providing each input data stream of the plurality of input data streams to the at least one output port based upon each corresponding recovered clock of the corresponding plurality of recovered clocks ([002], lines 1-12, each of the first and second serial data streams is clocked by the first and second recovered clocks, respectively).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ducaroir et al. (U.S. Pub. No. 2001/0043648) in view of Ziegler et al. (U.S. Pub. No. 2003/0112798).

Claim 1, Ducaroir discloses:

- first clock data recovery circuitry for receiving first serial data and recovering a first recovered clock from the first serial data ([0020], lines 17-18, 21-23);
- the transceiver provides the first recovered clock and a reference clock and the first serial data to a circuit portion of the transceiver ([0020], lines 14-16, 21-23);
- the circuit portion uses one of the first recovered clock and the reference clock for subsequent processing of the first serial data ([0020], the receiver is synchronized by the recovered clock where data is converted to parallel, transferred to the transmitter and where it is re-serialized with the reference clock).

Ducaroir fails to discloses a second clock data recovery circuitry for receiving second serial data and recovering a second recovered clock from the second serial data, wherein the transceiver provides the second serial data to the circuit portion and wherein the circuit portion uses one of the first recovered clock, the second recovered

clock and the reference clock for subsequent processing of one of the first and second serial data. However, Ziegler discloses circuitry for receiving a plurality of input serial data streams (Ziegler discloses receiving a first serial bit stream ([0021], lines 1-2 and receiving a second serial bit stream [0021], lines 4-5); clock data recovery circuitry for recovering a corresponding plurality of recovered clocks based on the plurality of input serial data streams; and logic for selecting from the plurality of input serial data streams and for providing at least one outgoing serial data stream to an outgoing transmit block (Ziegler discloses recovering a first recovered clock from the first serial bit stream [0023], lines 39-41 and recovering a second recovered clock from the second serial bit stream ([0023], lines 42-44); the transceiver provides the second serial data to the circuit portion and wherein the circuit portion uses one of the first recovered clock, the second recovered clock and the reference clock for subsequent processing of one of the first and second serial data ([0029], lines 5-8). Because Zeigler discloses that his serial data clock recovery and transmission method has the advantages of decreased cost and reduced data skew ([0005], lines 14-17), it would have been obvious to one skilled in the art at the time of invention to incorporate the serial data clock recovery and transmission method as disclosed by Zeigler into the invention of Ducaroir.

Claim 4, Ducaroir further discloses first serial data is an RX serial bit stream ([0020], lines 17-18).

13. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ducaroir et al. (U.S. Pub. No. 2001/0043648) and Ziegler et al. (U.S. Pub. No. 2003/0112798) as applied to claim 1 above, and further in view of Talbot (U.S. Pub. No. 2004/0014448). **Claim 3,** Ducaroir fails to discloses delay locked loop circuitry for receiving second serial data and produces a second recovered clock from the second serial data, wherein the transceiver provides the second serial data to the circuit portion and wherein the circuit portion uses one of the first recovered clock, the second recovered clock and the reference clock for subsequent processing of one of the first and second serial data. However, Ziegler discloses circuitry for receiving a plurality of input serial data streams (Ziegler discloses receiving a first serial bit stream ([0021], lines 1-2 and receiving a second serial bit stream [0021], lines 4-5); clock data recovery circuitry for recovering a corresponding plurality of recovered clocks based on the plurality of input serial data streams; and logic for selecting from the plurality of input serial data streams and for providing at least one outgoing serial data stream to an outgoing transmit block (Ziegler discloses recovering a first recovered clock from the first serial bit stream [0023], lines 39-41 and recovering a second recovered clock from the second serial bit stream ([0023], lines 42-44); the transceiver provides the second serial data to the circuit portion and wherein the circuit portion uses one of the first recovered clock, the second recovered clock and the reference clock for subsequent processing of one of the first and second serial data ([0029], lines 5-8). Because Zeigler discloses that his serial data clock recovery and transmission method has the advantages of decreased cost and reduced data skew ([0005], lines 14-17), it would have been obvious to one skilled in

the art at the time of invention to incorporate the serial data clock recovery and transmission method as disclosed by Zeigler into the invention of Ducaroir. Zeigler fails to disclose delay locked loop circuitry for receiving second serial data and produces a second recovered clock from the second serial data, However, Talbot discloses a clock recovery delay locked loop for providing a recover clock ([0066], lines 6-7). Because delay locked loops are well known in the art for clock recovery without the cost of hardware intensive oscillators, it would have been obvious to one skilled in the art at the time of invention to incorporate the delay locked loop as disclosed by Zeigler into the combined invention of Ducaroir and Zeigler.

14. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ducaroir et al. (U.S. Pub. No. 2001/0043648) and Ziegler et al. (U.S. Pub. No. 2003/0112798) as applied to claim 1 above, and further in view of Jordan et al. (U.S. 2004/0133734).

Claim 5, Although Ducaroir and Ziegler fail to disclose a programmable logic fabric for implementing these functions, Jordan discloses a programmable logic fabric portion ([0081], line 6). Jordan further discloses that the programmable logic fabric provides the advantage of flexibility in the configuration of functional models ([0081], lines 10-12). Because of this advantage it would have been obvious to one skilled in the art at the time of invention to incorporate the programmable logic fabric as disclosed by Jordan into the invention of Ducaroir.

15. Claims 10, 11, 12, 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ducaroir et al. (U.S. Pub. No. 2001/0043648) in view of Jordan et al. (U.S. 2004/0133734).

Claims 10, 14, Ducaroir discloses clock recovery circuitry coupled to receive a high data rate input data stream, wherein the clock recovery circuitry for recovers a recovered clock based on the high data rate input data stream ([0020], the receiver is synchronized by the recovered clock where data is converted to parallel, transferred to the transmitter and where it is re-serialized with the reference clock); and performs subsequent processing based on one of the recovered clock and a reference clock. Although Ducaroir fails to disclose a programmable logic fabric for implementing these functions, Jordan discloses a programmable logic fabric portion (Jordan, [0081]). Jordan further discloses that the programmable logic fabric provides the advantage of flexibility in the configuration of functional models ([0081], lines 10-12). Because of this advantage it would have been obvious to one skilled in the art at the time of invention to incorporate the programmable logic fabric as disclosed by Jordan into the invention of Ducaroir.

Claim 11, Ducaroir further discloses the high data rate input data stream is received according to a first protocol (serial data) and is converted to a second protocol (parallel) by the deserializer (performs a function, the programmable function fabric is disclosed by Jordan in Claim 10 above), based on the recovered clock ([0015], lines 1-4).

Claim 12, Ducaroir further discloses transmit circuitry coupled to receive the converted high rate input data stream in the second protocol, wherein the programmable logic

fabric portion provides the converted high data rate input data stream in the second protocol based on the recovered clock (transmit circuitry receives parallel data and uses recovered clock to convert to serial data for transmission, [0015], [0020]).

Claim 15, wherein the high data rate input data stream is received according to a first protocol (data received serially, [0015], lines 1-4).

Claim 16, the high data rate input data stream is converted to a second protocol based on the recovered clock (data converted to parallel using recovered clock, ([0015], lines 1-4).

16. Claims 13, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ducaroir et al. (U.S. Pub. No. 2001/0043648) and Jordan et al. (U.S. 2004/0133734) as applied to claims 11 and 16 above, and further in view of Ziegler et al. (U.S. Pub. No. 2003/0112798).

Claim 13, although neither Ducaroir nor Jordan discloses a second clock recovery circuit for recovering a second recovered clock based on an I/O serial data stream, Zeigler discloses recovering a second recovered clock from a serial bit stream ([0023], lines 42-44). Because Zeigler discloses that his serial data clock recovery and transmission method has the advantages of decreased cost and reduced data skew ([0005], lines 14-17), it would have been obvious to one skilled in the art at the time of invention to incorporate the serial data clock recovery and transmission method as disclosed by Zeigler into the combined invention of Ducaroir and Jordan.

Claim 17, although neither Ducaroir nor Jordan discloses the recovered clock is a first recovered clock, further comprising recovering a second recovered clock based on a transmitter clock. Because Zeigler discloses that his serial data clock recovery and transmission method has the advantages of decreased cost and reduced data skew ([0005], lines 14-17), it would have been obvious to one skilled in the art at the time of invention to incorporate the serial data clock recovery and transmission method as disclosed by Zeigler into the combined invention of Ducaroir and Jordan.

Claim 18, Zeigler further discloses transmitting the converted high data rate input data stream in the second protocol based on the second recovered clock ([0021]).

17. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziegler et al. (U.S. Pub. No. 2003/0112798) in view of Knapp et al. (U.S. Pub. No. 2005/0053179).

Claim 19, Ziegler discloses receiving a first serial bit stream ([0021], lines 1-2) and recovering a first recovered clock from the first serial bit stream ([0023], lines 39-41); receiving a second serial bit stream ([0021], lines 4-5) and recovering a second recovered clock from the second serial bit stream ([0023], lines 42-44); providing the first and second recovered clocks and a reference clock to a circuit portion ([0029], lines 5-8). Ziegler fails to disclose within the circuit portion, choosing among the first and second recovered clocks and the reference clock for subsequent processing. However, Knapp discloses choosing between a recovered clock and a reference clock for further signal processing ([0016], lines 21-23). Because clock selection allows better

synchronization of the data and clock, it would heave been obvious to one skilled in the art at the time of invention to incorporate the clock selection means as disclosed by Knapp into the invention of Ziegler.

Claim 20, Ziegler further discloses the first serial data is an RX serial bit stream (fig. 2, 226).

Claim 21, Ziegler further discloses the second serial bit stream is a TX serial bit stream (fig. 2, 244).

Allowable Subject Matter

18. Claim 23 is allowed.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. The examiner can normally be reached on M-F 1:00PM-9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571)272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Erin M. File

EF

1/27/2007

DAVID C. PAYNE
PRIMARY PATENT EXAMINER